

Exhibit F

Ex Parte Reexamination Interview Summary	Control No. 90/011,489	Patent Under Reexamination 6061520	
	Examiner ERIC B. KISS	Art Unit 3992	

All participants (USPTO personnel, patent owner, patent owner's representative):

- (1) ERIC B. KISS (3) Mary Steelman (USPTO)
(2) Fred Ferris (USPTO) (4) See continuation sheet

Date of Interview: 04 August 2011

Type: a) Telephonic b) Video Conference
c) Personal (copy given to: 1) patent owner 2) patent owner's representative)

Exhibit shown or demonstration conducted: d) Yes e) No.

If Yes, brief description: _____

Agreement with respect to the claims f) was reached. g) was not reached. h) N/A.

Any other agreement(s) are set forth below under "Description of the general nature of what was agreed to..."

Claim(s) discussed: 6.

Identification of prior art discussed: Lewis.

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:
See continuation sheet.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims patentable, if available, must be attached. Also, where no copy of the amendments that would render the claims patentable is available, a summary thereof must be attached.)

A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION MUST INCLUDE PATENT OWNER'S STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. (See MPEP § 2281). IF A RESPONSE TO THE LAST OFFICE ACTION HAS ALREADY BEEN FILED, THEN PATENT OWNER IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO PROVIDE THE MANDATORY STATEMENT OF THE SUBSTANCE OF THE INTERVIEW (37 CFR 1.560(b)). THE REQUIREMENT FOR PATENT OWNER'S STATEMENT CAN NOT BE WAIVED. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).

/ERIC B. KISS/ Primary Examiner, Art Unit 3992		
cc: Requester (if third party requester)		

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Interview Summary Continuation Sheet

All participants (USPTO personnel, patent owner, patent owner's representative):

(Continued from page 1)

- (4) Christopher Eide (Reg. No. 48,375)
- (5) Julia Akhter (Reg. No. 59,570)
- (6) Lissi Mojica (Reg. No. 63,421)
- (7) Tracy Druce (Reg. No. 35,493)
- (8) George Simion (Reg. No. 47,089)
- (9) Ben Goldberg

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

Parties discussed two features of claim 6: "play executing the code without running the code on the processing component to identify the operation if the code were run by the processing component," and, "creating an instruction for the processing component to perform the operation."

The examiners maintained that the "execution" using a simulated stack as disclosed by Lewis identifies the operations by recording information about constants, variable references, previously "executed" subexpressions, and procedure or method calls. Lewis at 126. Further, the examiners maintained that the generation of "good code" using the simulated stack values equates to creating an instruction. The examiner further indicated that the simulation described in Lewis appeared to be consistent with the simulation described in Code Table #5 of the '520 patent.

In response to the argument that Lewis does not disclose identifying only a single operation (as opposed to identifying multiple or even all operations), and generating only a single corresponding instruction (as opposed to generating multiple instructions), the examiners maintained that the claims are not limited to such.

/Eric B. Kiss/
Primary Examiner, CRU 3192

Reexamination Control No. 90/011,489
U.S. Patent No. 6,061,520; filed Apr. 7, 1988

Interview Agenda for August 4, 2011

I. **Claim Status**

- A. Claims 1-4, 8, 10, 12-17, 20, and 22 stand confirmed.
- B. Claims 6, 7, 9, 11, 18, 19, 21, and 23 stand rejected.
- C. Claim 5 is not subject to the reexamination.

II. **Claims 6, 7, 9, 11, 18, 19, 21, and 23 stand rejected under 35 U.S.C. 102(b) as being anticipated by Lewis. (B.T. Lewis et al., "Clarity MCode: A Retargetable Intermediate Representation for Compilation," ACM, IR '95, 1/95, San Francisco, California, USA, 1995.)**

A. Claim 6, for example, recites:

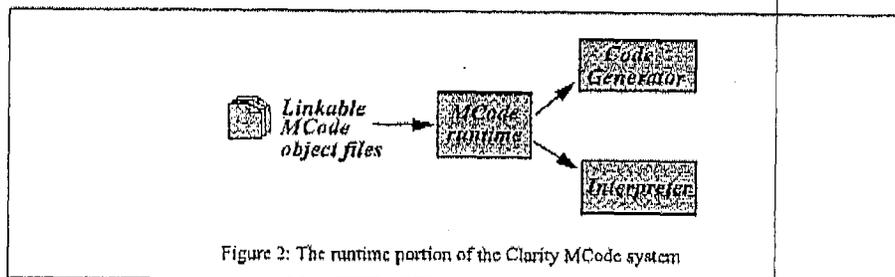
A method in a data processing system, comprising the steps of:
receiving code to be run on a processing component to perform an operation;
play executing the code without running the code on the processing component to identify the operation if the code were run by the processing component; and
creating an instruction for the processing component to perform the operation.

(Emphasis added.)

B. Background of Lewis

1. Lewis generally describes "Clarity C++ programming language," a dialect of C++ that was being developed by Sun Microsystems Laboratories around 1995. Lewis describes that code can be sent to a compiler and executed *or* the code can be sent to an interpreter (e.g., a virtual machine). For example, as illustrated in Figure 2, the MCode of Lewis follows one of two paths, to the "Code Generator" or to the "Interpreter." (Lewis at 121.)

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C. Lewis does not disclose or suggest at least the following elements of the independent claims (6 and 18)

1. Claim 6 recites:

- a) **“Play executing the code without running the code on the processing component to identify the operation if the code were run by the processing component,”** and
- b) **“creating an instruction for the processing component to perform the operation [as identified by the “play executing” process]”**

Claim 18 has similar recitations.

2. The acts performed by the compiler of Lewis fail to disclose or suggest anything similar to **“play executing”** of the code as specifically recited. In particular, Lewis discloses that MCode following the upper path of Figure 2 (reproduced herein) to **“Code Generator”** is compiled, but the process fails to disclose or suggest that this process in any way is done **“to identify the operation of the code if the code were run by the processing component.”**

3. The Office Action cites to page 126 of Lewis, which states:

The code generator ‘executes’ MCode instructions in order to maintain a running simulation of the MCode machine’s stack. Concrete subclasses of CGValue represent the state of the individual entries on the simulated stack. These entries include constants, variable references, previously ‘executed’ subexpressions, and procedure or method calls. The simulated stack records information about operands until the MCode instructions that use them are encountered. Machine code for (sub)expressions is only generated when the value of those expressions is needed.

(Lewis at 126.) (Emphasis added.)

This portion of Lewis describes that the **“simulated stack records information until MCode instructions that use them are encountered.”** In

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other words, "simulation of the MCode" is performed by the code generator to compile at least portions of the MCode into native machine code. This disclosure, despite using the terms "simulation" and "simulated," fails to disclose simulating or play executing the MCode as defined by the claims ". . . to identify the operation if the code were run by the processing component."

4. Further, Lewis clearly fails to disclose or suggest **"creating an instruction for the processing component to perform the operation [as identified by the "play executing" process]."** There is simply no disclosure in Lewis that an instruction is created for the processing component based on an identified operation from the "play executing" process. Again, the code generator outputs native machine code, but does not create an instruction to perform an identified operation.